



Controlling Noise and Radiation in Mixed-Signal and Digital Systems

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Good day, everyone. Welcome to this web-based presentation. Today we hope to help you understand some of the issues regarding noise and radiation in mixed-signal and digital systems, but this short seminar can not be an all-inclusive. The principles discussed here, combined with the engineering knowledge you already possess, will help you to produce designs with layouts that exhibit less noise and produce less radiation than many methods in current use.



Agenda

- **Signal Integrity and Line Termination**
- **Skin Effect**
- **Proximity Effect**
- **“Ground” Resistance**
- **Radiation**
- **Noise in the “Ground” System**
- **The Split Ground Plane Problem**
- **Improved Layout**
- **Summary of Rules**
- **Recommended Reading**



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Today's agenda will include some background information that will help you understand the principles upon which our recommendations are based. The discussion will include the principles relative to ADCs (analog-to-digital converters), but they apply just as well to all mixed signal circuitry and to high speed digital circuitry.

For your convenience, this presentation will be available for download from our web site and contains a Glossary of Terms at the very end.



Signal Integrity Problem

- **Signals propagate down a line**
- **Improper termination causes reflections**
- **Reflections**
 - Cause signal distortion
 - Cause signal radiation
- **Distortion**
 - Leads to a change in timing
 - Can lead to timing uncertainty (jitter)
 - Jitter causes ADC output noise



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High digital edge rates correspond to high frequencies and as digital rates increase and edges slew faster, it is becoming necessary to use high frequency, that is to say, analog, techniques in the design of printed circuit boards.

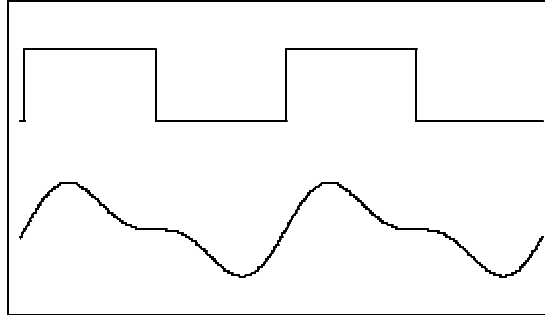
All lines carrying signals, digital or analog, are transmission lines, not just simple traces. We can often consider these lines to be simple traces and get away with it, but that can often be a dangerous consideration as far as the integrity of the signal is concerned.

Transmission lines, of course, need to be properly terminated to avoid signal reflections that can cause both distortion and radiation. The distortion, of course, can lead to a change of timing and jitter. The jitter, in turn, results in noise in the ADC conversion result.



Reflection Problem

- **Signals propagate down a line**
- **Improper termination causes reflections and signal distortion.**



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An improperly terminated signal line may distort that signal to the point that it does not go through an input threshold rapidly enough, resulting in uncertainty in the effective edge timing and in the interpretation as to whether it is a logic high or a low. For clock signals, this can result in misclocking. For an ADC clock, the result can be as mild as a noisy conversion result, or as serious as a complete malfunction.



When is Termination Needed?

- Simple traces need not be terminated
- Transmission Lines should be terminated
- Trace becomes a transmission line at:

$$\text{Length} \geq \frac{t_r}{6 \times t_{PR}}$$

Where t_r is the digital signal rise time
 t_{PR} is the signal propagation rate

Typical t_{PR} is about 150ps/inch on board of
FR-4 material



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Sometimes we can “get away” with treating a signal line as a simple trace. When must a trace be considered a transmission line? The formula here tells us that the line length beyond which a trace must be treated as a transmission line is a function of the digital signal rise time and the propagation rate across the board, but it is best to always treat the line as a transmission line.

For analog signals, it is common to use ¼ of the period of the highest frequency component of the signal in place of rise time.



Question: Is Termination Needed?



An ADC clock Signal has a 2ns rise time. The PCB is a typical one of FR-4 material. Beyond what line length should the line be properly terminated?

$$\text{Length} \geq \frac{t_r}{6 \times t_{PR}} = \frac{2 \times 10^{-9}}{6 \times 150 \times 10^{-12} / \text{in}}$$

$$\text{Maximum Length} = \frac{10^3}{450} = 2.2 \text{ inches (5.6 cm)}$$



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Here we consider an ADC clock with a 2ns rise time on a board of common FR-4 material. Answering this question is a simple matter of plugging the numbers into the equation on the previous page. The answer brings home the fact that a very short line can be a transmission line. Imagine the problem of very high frequency signals with sub-nanosecond rise times!



Termination Techniques

- **Two Types of Termination**
 - **Series – Matches Driver Output to Line**
 - $R_{\text{source}} + R_{\text{series}} = Z_0$
 - **A.C. – Matches Receiving end to Line**
 - **Series RC to Ground**



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There are two types of termination techniques. Series termination requires that a resistor be added in series with the line close to the signal source. The sum of the source resistance plus the added series resistor should equal the characteristic impedance of the line. This usually satisfies the termination requirements.

When series termination does not do the job, a.c. termination may be called for. The reason that series termination may not do the job usually results from using the single source to drive many loads, improper termination resistor value and/or a non-constant impedance of the line.

Causes of a non-constant line impedance include the use of feedthroughs on the line or other nearby lines with a non-constant distance from the line under question.



Series Termination

- **Series Termination: A Series Resistor**
 - Source Impedance + Resistor = Z_0
 - Resistor placed close to the source
- **Terminate When Source to Resistor Distance :**

$$\text{Length} \geq \frac{t_r}{6 \times t_{PR}}$$

NOTE: See National Semiconductor's Application Note AN-1113 (<http://www.national.com/an/AN/AN-1113.pdf>) for controlling line impedance.



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The driver output impedance plus the external series resistance should be equal to the characteristic impedance of the transmission line. The distance from the source to this resistor is limited by the same equation limiting the length of a simple trace. That equation is repeated here.

Implied here is the fact that the impedance of the line must be equal at all points. The further implication is that stripline or microstrip control techniques should be used. See National Semiconductor Application Note AN-1113 for more information.



A.C. Termination

- **A.C. Termination: Series RC to Ground at Destination**

- $R = Z_0$

- **C:**
$$C \geq \frac{4 \times t_{PR} \times L}{Z_0}$$

Where L is the line length

Z_0 is the characteristic impedance of the line

t_{PR} is the signal propagation rate down a board trace (about 150ps/inch with FR-4 board material)



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A.C. termination consists of a series RC from the line to ground, located near the destination pin but beyond it as seen from the signal source. The resistor value should be equal to the characteristic impedance of the line and the capacitor value is as indicated here. The units of t_{PR} and L should be consistent with each other.



Question (A.C. Termination)



A 7 inch long clock line with a 50-Ohm characteristic impedance need a.c. termination on an FR-4 board. What is the value of the series resistor and the smallest capacitor that should be used?

$$R = Z_0 = 50\Omega$$

$$C \geq \frac{4 \times t_{PR} \times L}{Z_0} \geq \frac{4 \times 150 \times 10^{-12} \times 7}{50} \geq 84 \text{ pF}$$



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Let's look at an example of a capacitor value for a.c. termination. The resistor value for a.c. termination should equal the characteristic impedance of the transmission line [1], or 50 Ohms in this case.

The minimum capacitor value is easily calculated to be 84 pF. A capacitor of 110 pF, 20% capacitor should do the job.



The Skin Effect

- **Current Seeks The Path of Least Impedance**
 - Entire Conductor at d.c.
 - Very Thin Skin Above a Few MHz
- **Inductance Causes Current to Flow on Skin**
- **Reduces Conductor Cross Sectional Area**
- **Increases Resistance**



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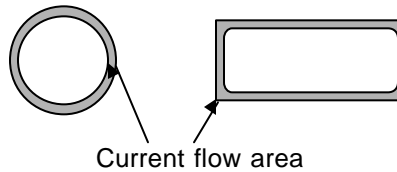
We have learned that current seeks the path of least resistance. The truth is that current seeks the path of least impedance. At d.c. they are the same, but circuit impedance can be quite a bit higher than circuit resistance at high frequencies. To make matters worse, a.c. resistance is higher than is d.c. resistance.

Since we are so accustomed to dealing with frequencies in the tens of Megahertz, we tend to regard "high" frequencies as something higher than this: perhaps a few hundred Megahertz or a Gigahertz. The fact remains, however, that high frequencies, as far as circuit impedances are concerned, are those frequencies beyond just a few Megahertz.

D.C. current flow fills the entire volume of a conductor, but a.c. current flow is restricted to the surface of a conductor because of the inductance of that conductor. This results in a lower effective conductor cross sectional area and increased a.c. resistance.



The Skin Effect: Skin Current



$$\text{Skin Depth} = \frac{2.6 * K}{\sqrt{f}}$$

$$K = \frac{1}{\mu_r} \cdot \sqrt{\frac{\rho}{\rho_{\text{Cu}}}}$$



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The skin effect is caused by the fact that the inductance in the center of a conductor is higher than it is on its surface. This results directly from the fact that the magnetic force radiates from the center of a conductor. The first "line of force" cuts through the entire conductor, but the very last line barely starts out from the center of the conductor before it is collapses. It never gets to the surface of the conductor. So, the surface of the conductor has fewer lines of force cutting it and less inductance than does the center of the conductor.

The result is that current flows almost exclusively on the surface of a conductor, reducing the effective cross section area of the conductor and increasing the conductor a.c. resistance. The conductor may as well be hollow as far as a.c. current flow is concerned.

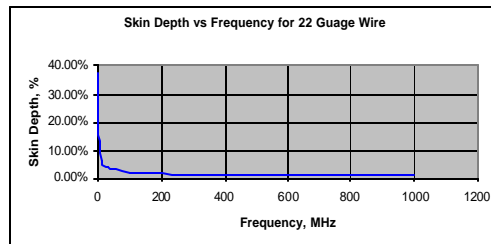
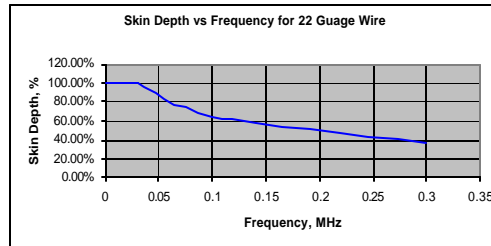
The average depth of current penetration, that is, the skin depth, is very shallow. The distribution of currents in a conductor experiencing the skin effect falls off exponentially as we approach the center of the conductor. The skin depth is as defined here, where μ_r is the magnetic permeability of the conductor relative to copper (so is 1 when the material is copper), ρ is the resistivity of the conductor, ρ_{Cu} is the resistivity of copper. For copper, $\rho/\rho_{\text{Cu}} = 1$ and k becomes unity.

The next slide shows a plot of skin depth as a percent of wire radius for 22 gauge wire.



Skin Depth vs Frequency

Freq (MHz)	Skin Depth, %
0.0003	100.00%
0.001	100.00%
0.003	100.00%
0.01	100.00%
0.03	100.00%
0.1	64.74%
0.3	37.38%
1	20.47%
3	11.82%
10	6.47%
30	3.74%
100	2.05%
300	1.18%
1000	0.65%



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The Skin Effect begins to take effect at about 42 kHz for 22 Gauge wire and Skin Depth falls off rather drastically as frequency increases. These plots show skin depth as a percentage of conductor radius. The lower plot goes from d.c. to 1 GHz. The upper plot shows detail only out to 300 kHz.



The Skin Effect: A.C. Resistance

The a.c. resistance of a conductor is much higher than its d.c. resistance.

$$R_{ac} = \frac{2.61 \times 10^{-7} \sqrt{f \times r_r}}{2 \times (w + h)}$$

where R_{ac} = AC resistance, Ohms/inch
f = frequency, Hz
 r_r = conductor relative resistivity, compared to copper = 1.00
w = flat trace width in inches
h = flat trace height or thickness in inches



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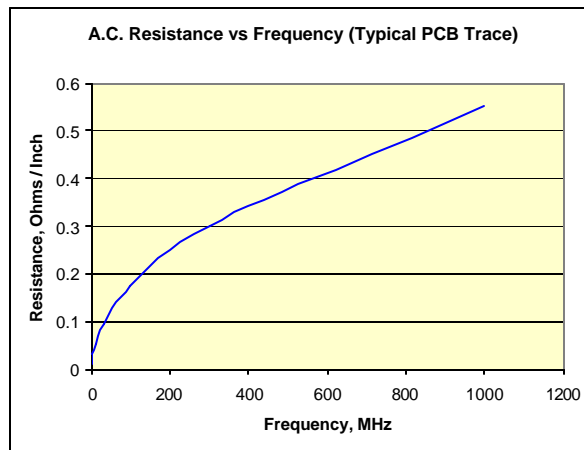
The formula here is for a flat conductor of width "w" and thickness "h".

The rapid falloff of skin depth with frequency tells us that the a.c. resistance increases rapidly at high frequencies. The a.c. resistance of a conductor at high frequencies, then, is much higher than is its d.c. resistance. The graph on the next slide illustrates this.



A.C. Resistance vs Frequency

PCB Trace 0.006" wide by 0.0015" high	
Freq, MHz	Rac
0.3	0.0095304
1	0.0174
3	0.0301377
10	0.0550236
30	0.0953037
100	0.174
300	0.3013768
1000	0.5502363



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As we see here, the skin effect really does have a big impact upon current flow. This is for a typical one ounce copper trace of 6 mills wide.



Question (A.C. Resistance)

?

What is the a.c. resistance in Ohms per inch at 80 MHz of a typical copper PCB trace that is 0.006 inch wide and 0.0015 inch thick?

$$R_{ac} = \frac{2.61 \times 10^{-7} \sqrt{f \times r_r}}{2 \times (w + h)} = \frac{2.61 \times 10^{-7} \sqrt{80 \times 10^6 \times 1}}{2 \times (0.006 + 0.0015)}$$

$$R_{ac} = \frac{2.61 \times 10^{-7} \sqrt{80 \times 10^6 \times 1}}{0.015} = \frac{0.00233}{0.015} = \underline{0.1556 \text{ Ohms/inch}}$$



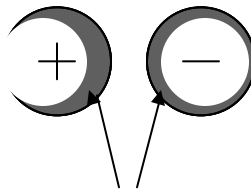
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Let's take a look at the a.c. resistance of a typical copper trace on a printed circuit board at 80 MHz. Since the trace is a copper one, ρ_r is unity. Substituting the frequency and trace dimensions in the equation reveals a resistance that is a real eye-opener!



Proximity Effect

The Proximity Effect on two conductors carrying opposite high frequency currents causes the a.c. current flow in those nearby conductors to be primarily on the side of the conductors nearest each other.



Current flow areas



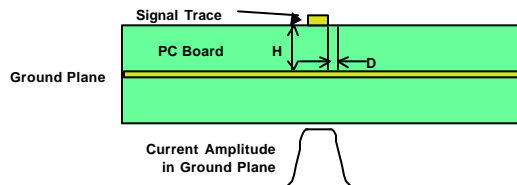
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As conductors come closer together, and/or as frequency increases, the current flowing through two adjacent conductors try to come closer to each other.

D.C. return currents will fill the entire conductor, where a.c. currents do not. The path of least impedance is the path where the magnetic fields around the outgoing and return currents are intimately bound together, causing these currents flow very close together. This causes ground plane currents to be pretty much confined to a path directly below the corresponding outgoing currents, as though the ground plane was really a return trace immediately below the outgoing line trace.



Proximity Effect on a PCB



$$I_{RP} = \frac{i}{H \times \pi \times (1 + (D/H)^2)} \text{ Amps/In}$$

where I_{RP} is the reference plane current density at horizontal distance "D" from the outgoing signal trace

i is the signal current

H is the height of the signal trace above the reference plane

D is the horizontal distance from the edge of the trace.



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The return current in the ground plane follows the outgoing current in the trace above (or below) it rather closely. The current at distance "D" from the edge of the trace falls to less than 4% of the current below the trace when the D/H ratio is 5 and to less than 1% of the current below the trace when the D/H ratio is 10. The result is a current density in the ground plane that is fairly well confined to the area below that current's corresponding outgoing current path.

The current density formula will tell us the current density at any point in the plane relative to the edge of the outgoing trace, or dimension "D". Note that this formula gives us current *density*, not just current.

Typical dimension "H" will depend upon which layers the trace and plane are located:

Between an outside layer and an inside layer "H" is typically 75 mills for 4-layer and 6-layer boards.

Between inside layers "H" is typically 39 mills for 4-layer board or 14 mills for 6-layer boards.



Ground Resistance

ADC Resolution (Bits)	ADC LSB Size (uV)	ADC Noise (LSB/Inch)	ADC Noise for 3 Inch Trace Length (LSB)
8	7813	0.07	0.2
10	1953	0.28	0.8
12	488	1.13	3.4
14	122	4.51	13.5
16	31	7.74	53.2

Ground plane resistance of 0.055 Ohms per inch (at 40 MHz) with an ADC reference voltage of 2.0 Volts can result in significant ground noise that can affect apparent ADC performance with as only 10mA_{P-P} of 40 MHz ground current.



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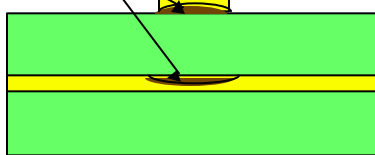
Here we see how 40 MHz noise in the ground plane can be significant. Note that, assuming 0.55 Ohms of ground path resistance, a three inch trace can produce enough ground noise to seriously affect high resolution ADCs. There is not much effect at 8 bits, but we can begin to see the effect at 10 bits. The noise can be prohibitive at 14 bits and higher.

You start to wonder if it is even possible to realize the full noise potential of a high speed, high resolution ADC.



Skin Effect + Proximity Effect

Current flows in a small area of the trace and reference plane.



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The skin effect and the proximity effect combine to limit the current carrying area of the conductor to a very small part of the conductor's cross sectional area. The areas of current flow are actually much smaller than shown here.



Radiation

- **Any Conductor Can**
 - Radiate
 - Pick Up Signals
- **Therefore, Any Conductor Can Be An Antenna**
- **Greater Loop Area Leads to a Better Antenna**
- **A Plane Can Radiate**
- **Copper With One Point Grounded can Radiate**



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As if the Skin Effect and the Proximity Effect were not enough, high frequency circuits carry yet another problem in the form of EMI. The problem is two-edged: signal radiation and signal pickup.

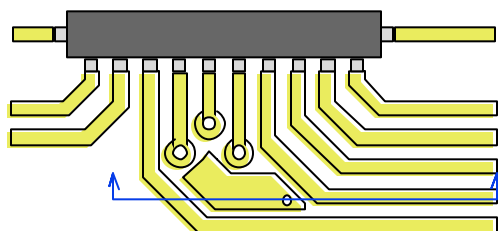
Governments of virtually all modern nations regulate the amount of interfering energy that can be radiated. This is good because it means there is less energy to be picked up by our circuits. However, we still must guard against our circuits radiating energy at unauthorized frequencies and good design practice also says we should design our circuits to resist pickup of interfering signals. After all, you never know when a circuit may be exposed to a high field environment.

When outgoing and return currents flow, there is a "loop area" that is defined by the area between the conductors. The larger this area is, the larger is the electromagnetic field "fringing" around the conductors. EM fringing is the cause of radiation, so larger loop areas will radiate and/or pick up more energy than will smaller loop areas. Since high frequency current flows in a restricted area of a ground plane, that path acts pretty much as a trace and can radiate, especially when the current path through the ground plane is forced to deviate from the outgoing current, as is most often the case with a split ground plane.

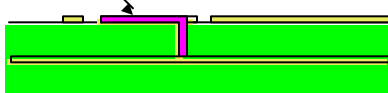
We tend to cover open areas on printed circuit boards with grounded copper. However, if we ground that copper area at a single point, we could create an antenna.



Built in Antenna



Antenna



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The rationale behind covering open areas with grounded copper is to get as much area as possible between ground plane and power plane. This will provide a high power plane to ground plane capacitance that is much more effective than is a physical capacitor. We do this because of the non-ideality of physical capacitors.

However, areas of copper that are grounded at only one point, as seen here, act as monopole or “whip” antennas.

Here we see a cross section of the printed circuit board as seen from the edge of the board if we cut it at the blue line. Can you locate the antenna? (2 to 3 second pause).

Any signal current that flows through the point in the ground plane where this grounded area is connected, and that is within the bandwidth of that antenna, is fed to that radiated by that antenna. Of course, the antenna is rather small, so it is may be harmonics of the ground plane energy that are radiated.

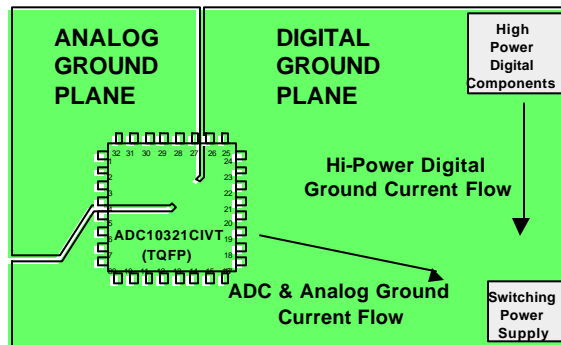
These antenna can also pick up electromagnetic field energy and feed that energy into the ground plane. Unless the field is very strong, however, there may not be enough energy to have a detrimental effect. Of course, you never know if your circuit might be subjected to a high field strength environment.

Using copper areas that are ungrounded altogether is also bad because not only do these isolated conductors serve no useful purpose, they can act as “directors” to focus and enhance signal energy or as “reflectors” to reflect signal energy back to a main antenna element, which may be another signal line.

The bottom line is that copper areas should neither be left floating nor should they be grounded at only a single point. Grounded copper areas should be connected to ground at rather close intervals, generally no more than about 1 inch spacing, forming a grid on the grounded surface.



Previous Suggestion



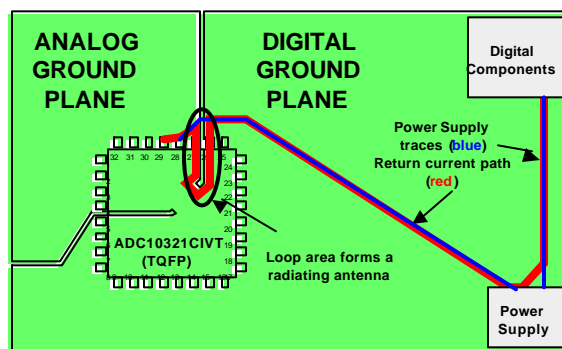
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We already alluded to the fact that the split ground plane can lead to problems when lines carrying signal currents cross the split between the planes. Of course, analog components will be kept in the analog area of the board and digital components in the digital area. This keeps analog and digital return currents away from each other. We have already seen that high frequency or high edge rate signals see a high resistance, even in a ground plane, so we know the need to keep analog and digital return currents separated from each other.

The layout shown here is one that I previously advocated and makes an attempt to isolate analog and digital ground currents, but ignores EMI effects. I have also found that this method works well up to 50 Msps for 10-bit ADCs and to about 30 to 35 Msps for 12-bit ADCs. Beyond that we see excessive circuit noise. The split ground plane can also lead to signal radiation, as we will see.



Loop Area Will Radiate

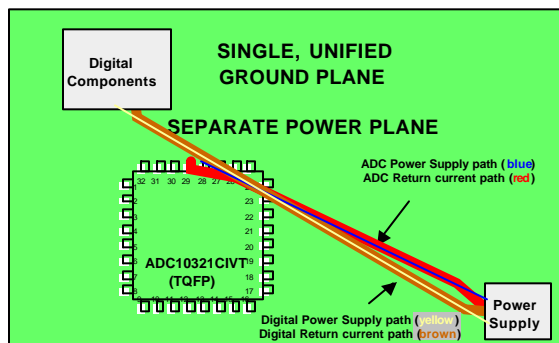


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Here is a board with a split ground plane, as I have previously advocated. It can be effective in limiting the path of ground currents to desired areas and minimizing ADC noise. However, the when we use supply traces to control the analog and digital power paths, we see that the return ADC current must deviate from the the outgoing current path. This produces a current loop area that can radiate.



Single Ground Plane and a Power Plane

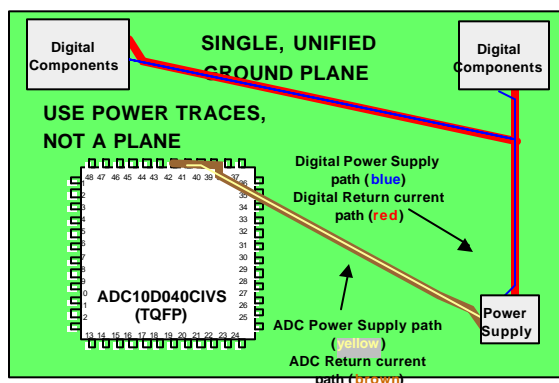


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We can eliminate the loop area problem and minimize the radiation problem by using both a ground plane and a power plane. This allows the outgoing and return currents to flow close to each other and minimize RFI/EMI problems. The problem now, however, is that component placement relative to other components is very important as common analog and digital return current paths can lead to digital noise in analog circuits.



Single Ground Plane, Power Traces, Careful Routing



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If we remember that the proximity effect causes outgoing and return currents to flow as close to each other as they can, we realize that we can control the path of return currents in the ground plane by careful component placement and thoughtful routing of all traces, including those of the power supply. Ground return currents will follow their respective outgoing traces and thus we can keep analog and digital return currents away from each other.

The single ground plane eliminates loop areas and the signal and power traces control current flow, even in the ground plane.

Analog and digital components should be located in their own, dedicated areas of the PC board. The power supply should be located at a board edge or corner and between analog and digital areas. Layout of power supplies can be critical for noise performance, but that is beyond the scope of today's presentation.

Digital components (especially high speed, high powered digital components) must not be placed on or near the path that analog return currents follow in getting back to the power supply. That is, they should not be located near lines carrying analog currents or power supply lines to analog or mixed-signal components.

Remember that power supply lines carry signal currents because they recharge bypass capacitors on the board. Their return currents must go through the common junction of a split ground plane, flowing away from the outgoing (power) trace/path. This forms a loop area that will radiate. Sometimes this radiation can be picked up by low level analog circuits.



Signal Traces vs. Transmission Line

- **“Long” Lines Are Not Traces**
- **Transmission Lines Can Distort Signals**
- **Distorted Digital Signals Produce:**
 - **Timing Uncertainty**
 - **Clock Jitter**
- **Through Hole Problem**
- **Layout Can Be Critical**



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Here is a brief review of some important points we have covered.

All signal carrying lines are transmission lines. Beyond a certain length we absolutely must treat them as such if we are to avoid signal distortion, timing problems and jitter.

Through holes in a transmission line create impedance discontinuities and cause reflections with their attendant distortion and noise problems. A through hole in a PCB has about 1 to 1½ nanoHenries of inductance, which can create problems. For example, at 14 Bits and 80 Msps, the ADC14080 (a coming 14-bit, 80 Megasamples per second ADC from National Semiconductor) will not tolerate bypass capacitors that are more than 2 to 3 millimeters from the bypassed pins. Putting these capacitors on the opposite side of the board results in the capacitors being isolated from the capacitors by the ¼ to ¾ Ohm (at 80 MHz) of the through hole inductance plus another ¼ Ohm or so in the trace inductance.

Layout is critical for transmission lines as they can experience impedance discontinuities when other lines approach them and depart from them. This is true even of the return current paths in the ground plane.



Maximum Trace Length

All traces are transmission lines, but a trace length longer than this absolutely must be treated as a transmission Line:

$$L_{MAX} = \frac{t_R}{6 \times t_{PD}}$$

where L_{MAX} is the maximum line length beyond which that line must be considered a transmission line

t_R is the signal rise time

t_{PD} is the signal propagation rate down the board



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We have shown that a PCB trace can become a transmission line at a surprisingly short distance. Digital rise time (NOT repetition rate or frequency) is what we use to determine maximum trace length before it must be considered a transmission line. For analog signals, we can use 1/4 of the period of the highest frequency component in the signal in place of rise time.



Summary of Rules

- **Use A Single, Unified Ground Plane**
- **Use Power Traces**
- **Let Trace Routing Control Ground Currents**
- **Keep Analog and Digital Power Traces Away From Each Other**
- **Tie Down Grounded Copper Areas at Many Points**
- **Remember: Traces Are Transmission Lines**



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Here is a summary of rules for maximizing high speed ADC and mixed signal performance. Much of this takes us back to what some of us learned in school but never used.



Recommended Reading

- ***High-Speed Digital Design, A Handbook of Black Magic*** by Howard W. Johnson and Martin Graham, Prentice-Hall, 1993 ISBN 0-13-395724-1
- ***Analog-Digital Conversion Handbook***, the Engineering Staff of Analog Devices, Inc, Prentice-Hall, edited by Daniel H. Sheingold, 1986, ISBN 0-13-032848-0



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The first book of our recommended reading should be in every engineer's library, whether she or he be an analog or a digital engineer. I feel this book should be entitled just *High-Speed Design* because the principles here apply to analog electronics as well. As a matter of fact, the principles are taken from analog electronics and applied to digital. The authors' premise is that they are presenting to digital engineers "what every analog engineer knows." While this may be true in general, not all of us analog engineers apply all of the principles presented in this book.

The second book used to be known as "the Blue Bible" of data conversion products and systems. While it has some great information, it is somewhat outdated and lacking current information. It is, however, a good book for understanding fundamental ADC and DAC principles and (some) specifications.



National Semiconductor Data Converter Web Site

- **National Semiconductor's Data Conversion web site:** www.national.com/adc

- Application Notes
- Data Conversion Calculator
- Definitions of Terms (ADC / DAC)
- Evaluation Boards, Manuals, Software
- Press Releases
- Selection Guides
- Technical Articles
- Technical Presentations
- Technical Support Link



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National Semiconductor is just as committed to providing useful information to our customers as we are to providing leading edge solutions in silicon. Visit our Data Conversion web site for a lot of useful information. Check out this web site periodically as we are continually adding to it and making improvements to it.

We believe we have an extremely useful website. Visit us then click on "Feedback" at the bottom of the page and let us know what you think. Please be sure to mention that it is the ADC web site about which you are making comments. We welcome all feedback, positive and negative, that will help make this site more useful for you.

Some of the very useful things there include a Data Conversion Calculator where you can determine relationships between various dynamic parameters and determine the minimum resolution needed for a given performance level. The Definition of Terms will help take the mystery out of specifications.

Our evaluation boards and WaveVision™ software provide the easiest means available to evaluate the performance of our ADCs.

The technical articles and presentations can offer help in gaining more design knowledge.

The technical support link serves to get your technical questions answered. Of course, you can also contact your distributor and ask to speak with an applications engineer if you need technical assistance.

www.national.com/adc

National High-speed ADCs

Part Number	Res. (Bits)	Supply (V)	Power (mW)	Vin (Vpp)	Speed (MSPS)	Static Perf.		Dynamic Characteristics			
						INL (lsb)	DNL (lsb)	ENOB (Bits)	SINAD (dB)	THD (dB)	SFDR (dB)
ADC1173	8	3	33	2	15	+/-0.5	+/-0.4	7.6	48	-54	55
ADC1175	8	5	60	2	20	+/-0.5	+/-0.35	7.3	46	-57	58
ADC1175-50	8	5	125	2	50	+/-0.8	+/-0.7	6.7	42	-54	56
ADC08351	8	3	36	2	42	+/-0.7	+/-0.6	6.8	43	-46	49
ADC08060	8	3	78	1.6	60	+/-0.5	+/-0.4	7.1	44.5	-63	63
ADC08L060	8	3	39	2	60	+0.5/-0.2	+/-0.25	7.6	43.3	-57	59.1
ADC08100	8	3	130	1.6	100	+/-0.5	+/-0.4	7.0	43.9	-60	60
ADC08200	8	3	210	2	200	+/-1.0	+/-0.4	7.3	46	-60	60
ADC08D060*	8	1.2	2.1W	1.6	800	+/-0.5	+/-0.5	7.5	47	-58	62
ADC10221	10	5	98	2	15	+/-0.45	+/-0.35	9.5	59	-70	72
ADC10321	10	5	98	2	20	+/-0.45	+/-0.35	9.5	59	-70	72
ADC10030	10	5	125	2	30	+/-0.45	+/-0.40	9.4	58	-66	68
ADC10D020	10, dual	3	150	2 (Diff)	20	+/-0.65	+/-0.35	9.5	59	-73	75
ADC10D040	10, dual	3.3	267	2 (Diff)	40	+/-0.65	+/-0.35	9.1	59	-69	72
ADC12081	12	5	105	2	5	+/-0.6	+/-0.35	10.9	67.6	-79	79
ADC12181	12	5	235	2	10	+/-0.7	+/-0.4	10.4	64.5	-74	73
ADC12281	12	5	443	2	20	+/-1.0	+/-0.35	10.5	65	-76	75
ADC12010*	12	5	180	2 (Diff)	10	+/-0.7	+/-0.4	11.2	69	-80	86
ADC12040	12	5	340	4 (Diff)	40	+/-0.7	+/-0.4	11.2	69	-80	84
ADC12D040	12, dual	3	600	4 (Diff)	40	+/-0.7	+/-0.4	10.9	68	-78	80
ADC12L063	12	3.3	354	2 (Diff)	62	+/-1.0	+/-0.5	10.6	62	-74	78
ADC12L066	12	3.3	354	2 (Diff)	66	+/-1.0	+/-0.5	10.6	65	-74	78
ADC12DL066*	12, dual	3	600	2 (Diff)	66	+/-0.7	+/-0.4	10.5	68	-74	78
CLC5957	12	5	640	2 (Diff)	70	+/-1.5	+/-0.05	10.5	65.5	-71	74
ADC12L080*	12	3	430	2 (Diff)	80	+/-1.2	+/-0.4	10.2	66	-72	80
ADC14161/061	14	5	390	2 (Diff)	2.5	+/-0.75	+/-0.3	12.8	79	-88	90
ADC14071	14	5	380	2 (Diff)	7	+/-2.2	+/-0.6	12.6	77	-83	90
ADC14080*	14	5	1.5W	2 (Diff)	80	+/-1.5	+/-0.5	12	74	-92	90
ADC16061	16	5	390	2 (Diff)	2.5	+/-3.0	+/-1.0	12.8	79	-88	92

* Preliminary Products, Specifications subject to change

Eval Boards Available for all released High Speed ADCs
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This is a summary table of National Semiconductor's current High Speed ADC offerings, as well as some products, in red, that are coming. This table only shows high speed ADCs, but we have lower speed products and will be expanding our lower speed offering and adding more DACs to our portfolio.

National is committed to the data conversion business. Watch for future offerings.



Summary

- **Signal Integrity**
- **Skin Effect**
- **Proximity Effect**
- **“Ground” Resistance**
- **Radiation**
- **Grounding of Open Areas**
- **Noise in the “Ground” System**
- **The Split Ground Plane Problem**
- **Use Power Traces and Thoughtful Layout**
- **Summary of Rules**
- **Recommended Reading**



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This presentation discussed some concepts that are generally considered part of the analog world, but can have impact in digital areas as well. We did not exhaust the subject by any means. The material here is very basic and introductory in nature. Also, there are other effects that we did not discuss. For example, power supply bypassing is a rather big area that most of us consider trivial. But, that is another subject. We presented some questions throughout the presentation to help solidify the principles in your minds.

This presentation will be available on our web site and includes a Glossary of Terms that should prove useful as you do some self-study in this area.



Thank you for attending our seminar. We will now answer any questions that have not already been addressed.



Glossary of Terms

A.C. Termination – Transmission line termination technique where a series RC is used at the receiving end of a transmission line.

ADC – Analog-to-Digital Converter. A device or circuit used to convert analog information to digital words.

ADC10D040 – A 10-bit, 40 Msps (Megasample per second) ADC

ADC12040 – A 12-bit, 40 Msps (Megasample per second) ADC

ADC14080 – A 14-bit, 80 Msps (Megasample per second) ADC

DAC – Digital-to-Analog Converter. A device or circuit used to convert digital words into analog voltages or currents.

Characteristic Impedance - The impedance a transmission line such that, when driven by a circuit with that output impedance, the line appears to be of infinite length such that it will have no standing waves, no reflections from the end and a constant ratio of voltage to current at a given frequency at every point on the line.

Director – The shorter elements of a “Yagi” antenna that directs energy toward the driven element.

FFT – Fast Fourier Transform. Most of us relate the FFT to the FFT plot of frequency vs. amplitude.

EMI/RFI – Electromagnetic Interference/Radio Frequency Interference. This is the radiation of EM (electromagnetic) energy that may interfere with other circuits and systems.

FR-4 – A glass epoxy printed circuit board material of woven glass cloth construction laminate with an epoxy resin binder.

Full-Scale Input Swing – The difference between the maximum and minimum input voltages that will produce a valid ADC output without going over- or under-range.

Gain Error - The error in the slope of the ADC transfer characteristic. It is the difference in the actual and ideal full scale input range values.

Input Dynamic Range – For an ADC, the range of voltages that can be applied to the input without going under or over range.

Jitter - The cycle-to-cycle variation in the timing of a signal.

Loop Area – The area between the conductors of outgoing and return currents.

LSB – Least Significant Bit. The bit that has the least weight.

Offset Error – For an offset binary ADC, this is of how far the mid-scale transition point is from the ideal zero voltage input. For a single ended input ADC, this how far the first code transition point is from the ideal $\frac{1}{2}$ LSB input voltage.

PC Board – Printed Circuit Board.

PCB – Printed Circuit Board.

Proximity Effect – The phenomenon whereby outgoing and return currents want to flow close to each other.

PSRR – Power Supply Rejection Ratio of an ADC. DC PSRR is the ratio of the the change in some specified parameter to a change in the power supply voltage. AC PSRR is the ratio of the output level of some frequency riding on the power supply to the peak-to-peak level of that signal at the power supply, normalized to the ADC full scale range.

Reflector – The longer elements of a “Yagi” antenna that reflect energy back to the driven element.

Resolution – The number of discrete output states or values of an ADC or a DAC, Can also be expressed in the number of digital bits in the output (for ADCs) or the input (for DACs).

Sampling Noise – The inherent noise of an ADC that comes from the steps in the transfer function.

Scale Factor – The effective multiplier of the analog reference voltage input to an ADC or DAC. This value is usually one, but can be any whole or fractional number.

Series Termination - Adding a resistor in series with a transmission line such that the driver output impedance plus the resistance of this external resistor is equal to the characteristic impedance of the transmission line.

Skin Effect – The phenomenon by which high frequency current flow is restricted to the surface, or skin, of a conductor.

SNR – Signal-to-Noise Ratio is the ratio of the power in the signal to the power in all other spectral components, except the harmonics and d.c.

Split Ground Plane – Concept where analog and digital grounds are in a single PCB layer and only connected at a single point.

Substrate – The base semiconductor material upon with solid state devices are built. The substrate is resistive with a resistance that is on the order of a few Ohms.

Through Hole – The hole that goes through a printed circuit board to connect together lines and/or planes in two or more layers

Z_0 – The characteristic impedance of a transmission line