

Active Errata List

- USB – Ping-Pong databank 1 Re-transmission Failure
- USB – Ping-Pong OUT Bad Reception
- USB – Bad Remote Wake-up Generation
- UART Interface – During Reception, Clearing REN may Generate Unexpected IT
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- Timer 2 – Baud Rate Generator – Long Start Time

Errata History

Lot Number	Errata List
A5560 or above	1, 2, 3, 4, 5, 6, 7, 8, 9

Errata Description

1. USB – Ping-Pong Databank 1 Re-transmission Failure

When the host does not acknowledge an IN data packet from the databank 1 of a ping-pong endpoint, the endpoint retry-mechanism sends corrupted data.

Workaround

None.

2. USB - Ping-Pong OUT Bad Reception

When the host sends a packet with a size lower than the size defined in the DPRAM endpoint (Ping-Pong Only), there is a risk of having a corrupted packet in the DPRAM with a wrong number of bytes reported. This problem occurs only in Ping-Pong mode if the 2 banks are full and bank 1 is cleared when the host is sending a packet at that time. If the packets are of the size of the DPRAM endpoint, there is no problem even in Ping-Pong mode.

If the device application software is quick enough to read the received packets to avoid the case where the 2 banks are full, there is no problem even if the packet sizes are not of the same size of the DPRAM endpoint.

Workaround

None.

3. USB - Bad Remote Wake-up Generation

The remote wake-up generates an SE0 and J state (at the end of the Upstream Resume K) that are reserved by the Host.

Workaround

None.

4. UART Interface – During Reception, Clearing REN may Generate Unexpected IT

During UART reception, if the REN bit is cleared between start bit detection and the end of reception, the UART will not discard the data (RI is set).



USB Microcontrollers

AT89C5131

Errata Sheet



Workaround

Test REN bit at the beginning of interrupt routine just after CLR RI, and run the Interrupt routine code only if REN is set.

5. C51 Core – Power-down Exit Failure in X2 Mode

If CPU is configured in X2 mode when exiting from power down, the first address fetched may be lost

Workaround Two solutions are possible:

- a) Set CPU in X1 mode before entering in power-down mode and then restore CPU to X2 mode when the CPU is woken up.
- b) Add a NOP (0x00) opcode just after the instruction which activates the power down mode. As this NOP is randomly non executed, the behavior of the software is correct.

Example:

```
MOV PCON, #02H; Power down mode activation
```

```
NOP      ; This NOP is randomly not executed
```

```
..... ; Put here the first opcode to execute after exiting from power down mode
```

6. Timer 0/1 – Unexpected Interrupt

If one of the timers 0 and 1 is in X1 mode while the other one is in X2 mode, an unexpected interrupt may randomly occur for one of the timers.

Workaround

Use the same mode X1 or X2 for both timers. This condition is met if PLL is used to clock the CPU.

7. USB Interface – CPU Wake-up Interrupt Not Cleared if CPU Frequency Greater or Equal to 12 Mhz/X2

The WUPCPU bit in USBINT register is set by the hardware when the USB macro exits from suspend mode. The firmware acknowledges this event by clearing the WUPCPU bit in the interrupt routine. If the CPU frequency is greater or equal to 12 MHz/X2, the WUPCPU bit is cleared in the USBINT register but not in the USB macro. Therefore the next time the USB macro exits from suspend mode, the WUPCPU bit is not set by the hardware and the CPU fails to exit from the power down mode.

Workaround

None

8. USB Interface – Data Corruption in Endpoint0 and FIFO

Data in Control Endpoint and FIFO may be corrupted if USB macro and CPU write simultaneously in. This condition occurs if the host cancels a control IN transaction with premature OUT and sends the following SETUP while the C51 is writing into the FIFO instead of the cancellation.

Workaround: There are two ways to avoid this problem.

- a) Use 32 bytes FIFO
- b) Test NAKIN and NAKOUT bits to know which way the communication is performed. Once the data has been transferred, the firmware clears the TXCMPL bit and the NAKIN bit. If the NAKIN bit is set by the hardware, this means that the host asks for more data. If the RXOUT bit is set by the hardware, this means that the host has already sent the status stage and no longer asks for data.

9. Timer 2 – Baud Rate Generator – Long Start Time

When Timer 2 is used as a baud rate generator, TH2 is not loaded with RCAP2H at the beginning, then UART is not operational before 10,000 machine cycles.

Workaround

Add the initialization of TH2 and TL2 in the initialization of Timer 2.



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