AVR32715: AVR32 UC3B Schematic Checklist

Features

- **Power circuit**
- **Reset circuit**
- **USB connection**
- **ABDAC sound DAC interface**
- **JTAG and Nexus debug ports**
- **Clocks and crystal oscillators**

1 Introduction

A good hardware design comes from a proper schematic. Since UC3B devices have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when starting and reviewing the schematics for a UC3B design.

32-bit AVR® Microcontrollers

Application Note

Rev. 32095D-AVR32-12/08

2 Power circuit

2.1 Single 3.3 volt power supply

Figure 2-1. Single 3.3 volt power example schematic

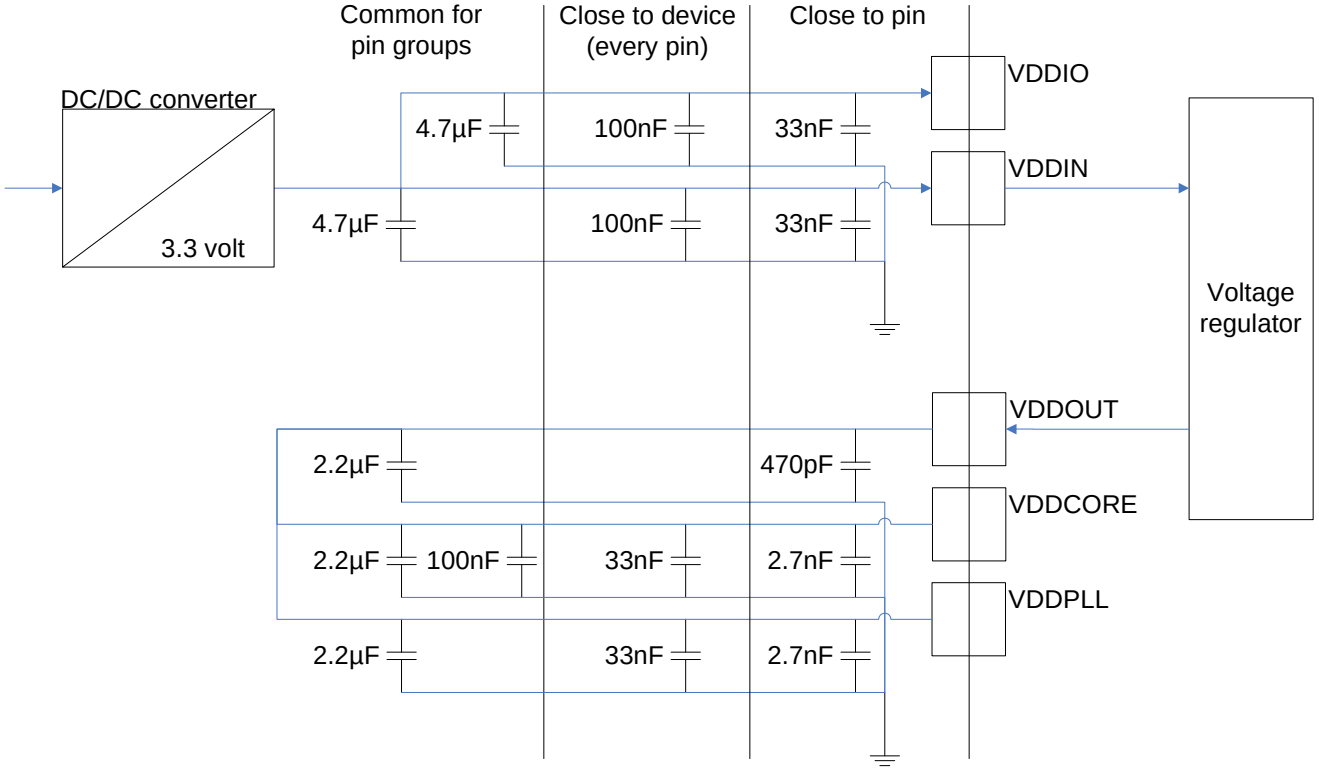

Table 2-1. Single 3.3 volt power supply checklist

☑	Signal name	Recommended pin connection	Description
	VDDIO	3.0 V to 3.6 V Decoupling/filtering capacitors 33 nF[(1)(2)], 100 nF[(1)(3)] and 4.7 µF[(1)]	Powers I/O lines and USB transceiver. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDIN	3.0 V to 3.6 V Decoupling/filtering capacitors 33 nF[(1)(2)], 100 nF[(1)(3)] and 4.7 µF[(1)]	Powers on-chip voltage regulator. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDOUT	Decoupling/filtering capacitors 470 pF[(1)(2)] and 4.7 µF[(1)]	Output of the on-chip 1.8V voltage regulator. Decoupling/filtering capacitors must be added to guarantee 1.8V stability.

☑	Signal name	Recommended pin connection	Description
	VDDCORE	1.65 V to 1.95 V Connected to VDDOUT Decoupling/filtering capacitors 2.7 nF(1)(2), 33 nF(1)(3), 100 nF(1) and 4.7 µF(1)	Powers device, flash logic and on-chip RC. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDPLL	1.65 V to 1.95 V Connected to VDDOUT Decoupling/filtering capacitors 2.7 nF(1)(2), 33 nF(1)(3) and 4.7 µF(1)	Powers the main oscillator and the PLL. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.

Note 1: These values are given only as a typical example.

Note 2: Decoupling capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

Note 3: Decoupling capacitor should be placed close to the device for each pin in the signal group.

2.2 Dual 3.3 volt and 1.8 volt power supply

Figure 2-2. Dual 3.3 volt and 1.8 volt power example schematic

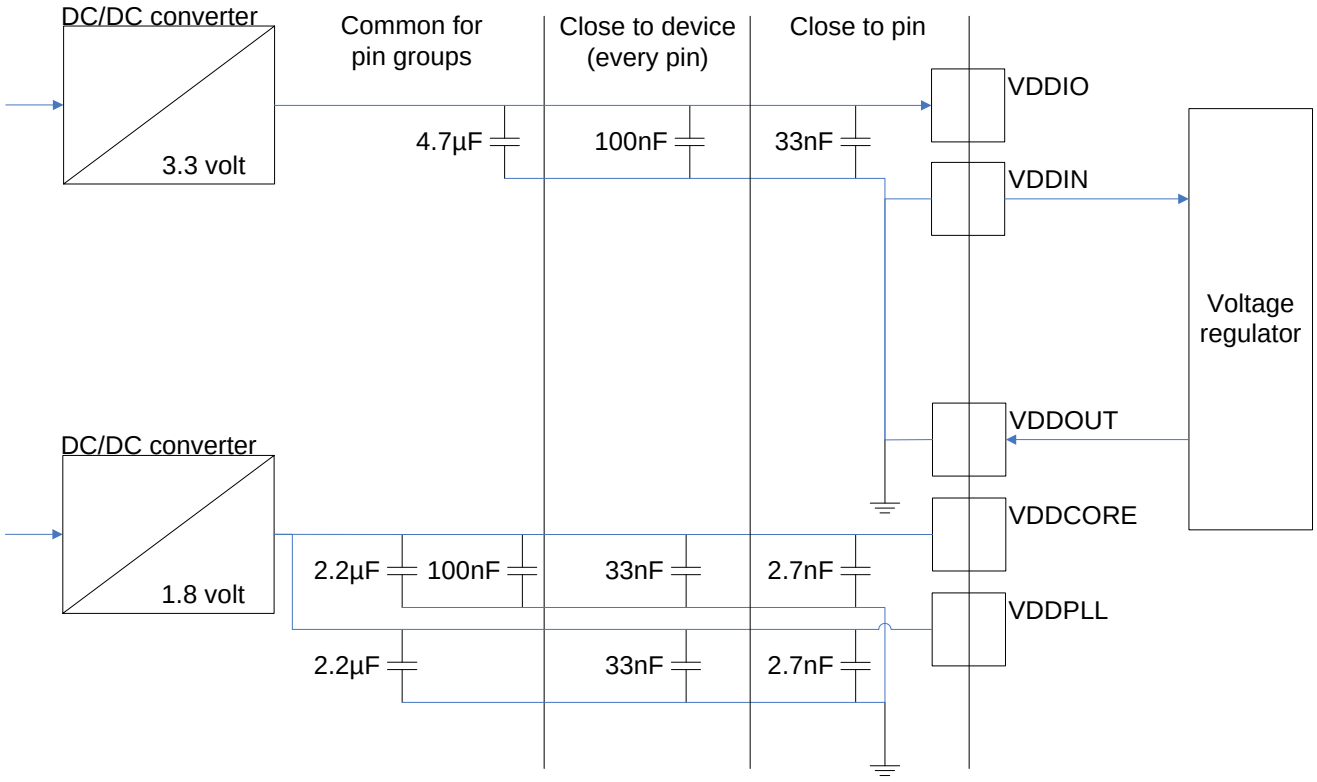

Table 2-2. Dual 3.3 volt and 1.8 volt power supply checklist

☑	Signal name	Recommended pin connection	Description
	VDDIO	3.0 V to 3.6 V Decoupling/filtering capacitors 33 nF(1)(2), 100 nF(1)(3) and 4.7 µF(1)	Powers I/O lines and USB transceiver. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDIN	Connected to ground	On-chip voltage regulator not in use.

☑	Signal name	Recommended pin connection	Description
	VDDOUT	Connected to ground	On-chip voltage regulator not in use.
	VDDCORE	1.65 V to 1.95 V Decoupling/filtering capacitors 2.7 nF(1)(2), 33 nF(1)(3), 100 nF(1) and 2.2 µF(1)	Powers device, flash logic and on-chip RC. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDPLL	1.65 V to 1.95 V Decoupling/filtering capacitors 2.7 nF(1)(2), 33 nF(1)(3) and 2.2 µF(1)	Powers the main oscillator and the PLL. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.

Note 1: These values are given only as a typical example.

Note 2: Decoupling capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

Note 3: Decoupling capacitor should be placed close to the device for each pin in the signal group.

2.3 ADC reference power supply

The following schematic checklist is only necessary if the design is using the internal analog to digital converter.

Figure 2-3. ADC reference power supply example schematic

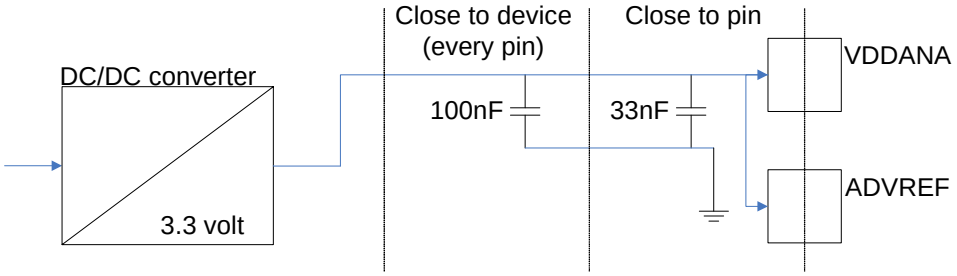

Table 2-3. ADC reference power supply checklist

☑	Signal name	Recommended pin connection	Description
	VDDANA	3.0 V to 3.6 V Decoupling/filtering capacitors 33 nF(1)(2) and 100 nF(1)(3)	Powers on-chip ADC. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	ADVREF	2.6 V to VDDANA Connect with VDDANA	ADVREF is a pure analog input.

Note 1: These values are given only as a typical example.

Note 2: Decoupling capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

Note 3: Decoupling capacitor should be placed close to the device for each pin in the signal group.

2.4 No ADC power supply

The following schematic checklist is only necessary if the design is not using the internal analog to digital converter.

Figure 2-4. No ADC power supply example schematic

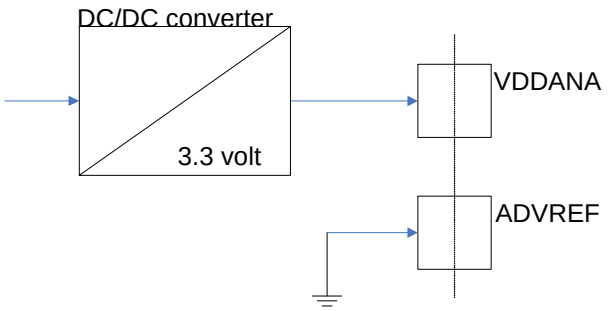

Table 2-4. No ADC power supply checklist

☑	Signal name	Recommended pin connection	Description
	VDDANA	3.0 V to 3.6 V	
	ADVREF	Connected to ground	

3 Reset circuit

Figure 3-1. Reset circuit example schematic

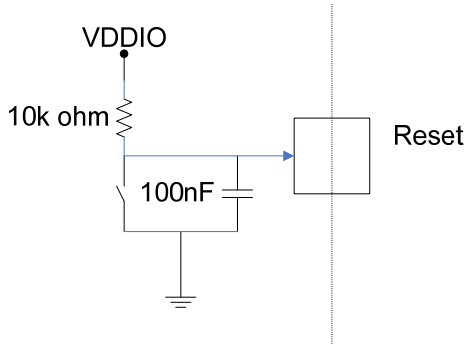

Table 3-1. Reset circuit checklist

☑	Signal name	Recommended pin connection	Description
	RESET	Can be left unconnected in case no reset from the system needs to be applied to the product	The RESET_N pin is a Schmitt input and integrates a permanent pull-up resistor to VDDIO.

4 Clocks and crystal oscillators

4.1 External clock source

Figure 4-1. External clock source schematic

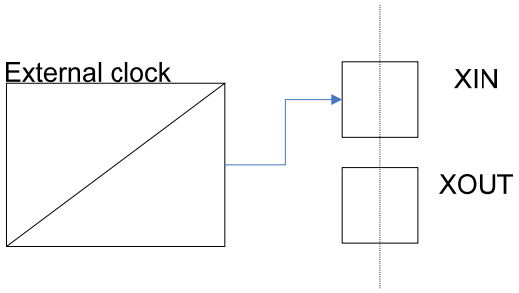

Table 4-1. External clock source checklist

☑	Signal name	Recommended pin connection	Description
	XIN	Connected to clock output from external clock source	Up to VDDIO volt square wave signal up to 50 MHz.
	XOUT	Can be left unconnected or used as GPIO	

4.2 Crystal oscillator

Figure 4-2. Crystal oscillator example schematic

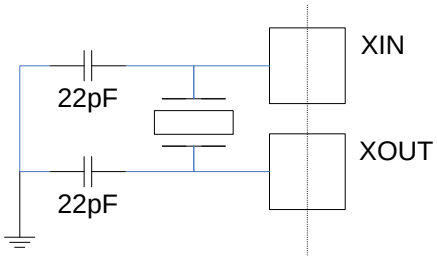

Table 4-2. Crystal oscillator checklist

☑	Signal name	Recommended pin connection	Description
	XIN	Biasing capacitor 22 pF[(1)(2)]	External crystal between 450 kHz and 16 MHz.
	XOUT	Biasing capacitor 22 pF[(1)(2)]	

Note 1: These values are given only as a typical example. The capacitance C of the biasing capacitors can be computed based on the crystal load capacitance C_L and the internal capacitance C_i of the MCU as follows:

$C = 2 (C_L – C_i)$

The value of C_L can be found in the crystal datasheet and the value of C_i can be found in the MCU datasheet.

Note 2: Decoupling capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

5 USB connection

5.1 Device mode, powered from bus connection

Figure 5-1. USB in device mode, bus powered connection example schematic

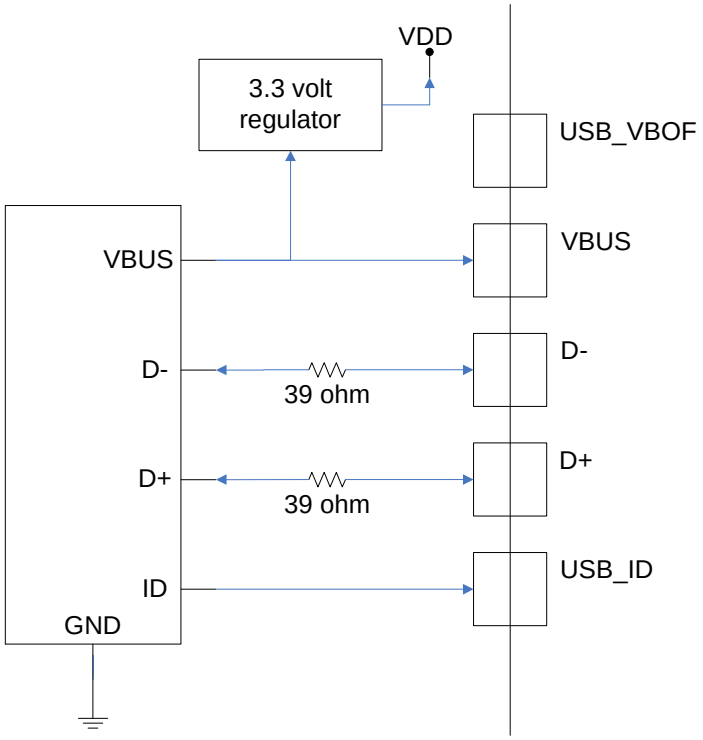

Table 5-1. USB bus powered connection checklist

☑	Signal name	Recommended pin connection	Description
	USB_VBOF	Can be left unconnected	USB power control pin.
	VBUS	Directly to connector	USB power measurement pin.
	D-	39 ohm series resistor Placed as close as possible to pin	Negative differential data line.
	D+	39 ohm series resistor Placed as close as possible to pin	Positive differential data line.
	USB_ID	Can be left unconnected	Mini connector USB identification pin.

5.2 Device mode, self powered connection

Figure 5-2. USB in device mode, self powered connection example schematic

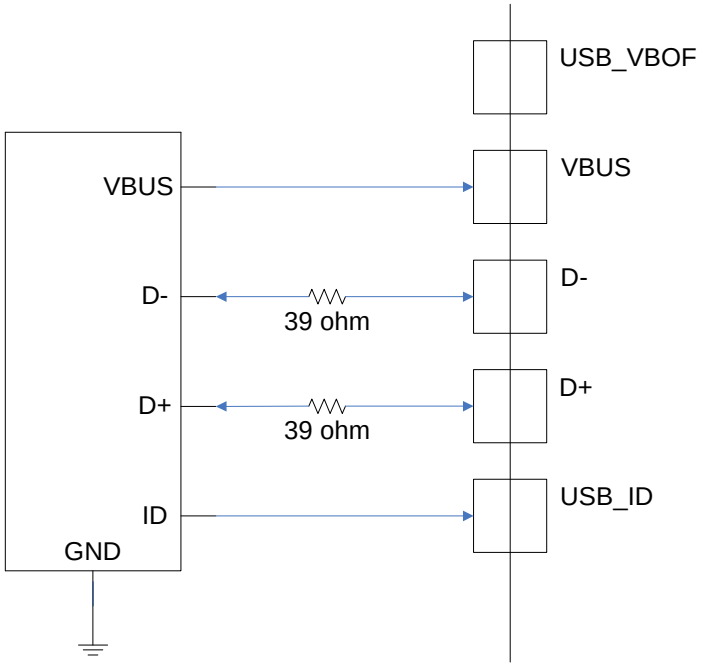

Table 5-2. USB self powered connection checklist

☑	Signal name	Recommended pin connection	Description
	USB_VBOF	Can be left unconnected	USB power control pin.
	VBUS	Directly to connector	USB power measurement pin.
	D-	39 ohm series resistor Placed as close as possible to pin	Negative differential data line.
	D+	39 ohm series resistor Placed as close as possible to pin	Positive differential data line.
	USB_ID	Can be left unconnected	Mini connector USB identification pin.

5.3 Host/OTG mode, power from bus connection

Figure 5-3. USB host and OTG powering connection example schematic

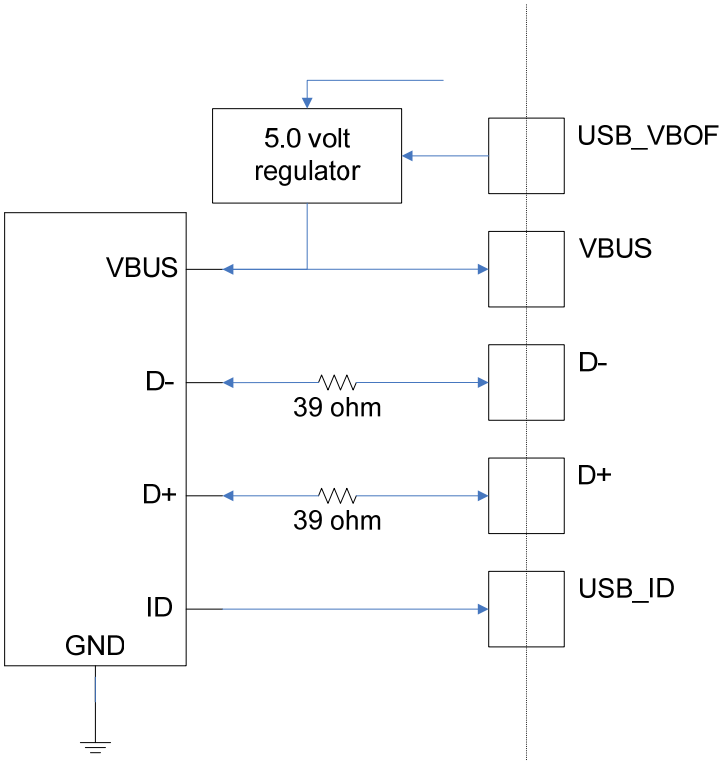

Table 5-3. USB host and OTG powering connection checklist

☑	Signal name	Recommended pin connection	Description
	USB_VBOF	GPIO connected to VBUS 5.0 volt regulator enable signal	USB power control pin.
	VBUS	Directly to connector	USB power measurement pin.
	D-	39 ohm series resistor Placed as close as possible to pin	Negative differential data line.
	D+	39 ohm series resistor Placed as close as possible to pin	Positive differential data line.
	USB_ID	GPIO directly connected to connector, mandatory in OTG mode	Mini connector USB identification pin. For OTG it will be tied to ground in host mode, and left floating in device mode. Pull-up on GPIO pin must be enabled.

6 JTAG and Nexus debug ports

6.1 JTAG port interface

Figure 6-1. JTAG port interface example schematic

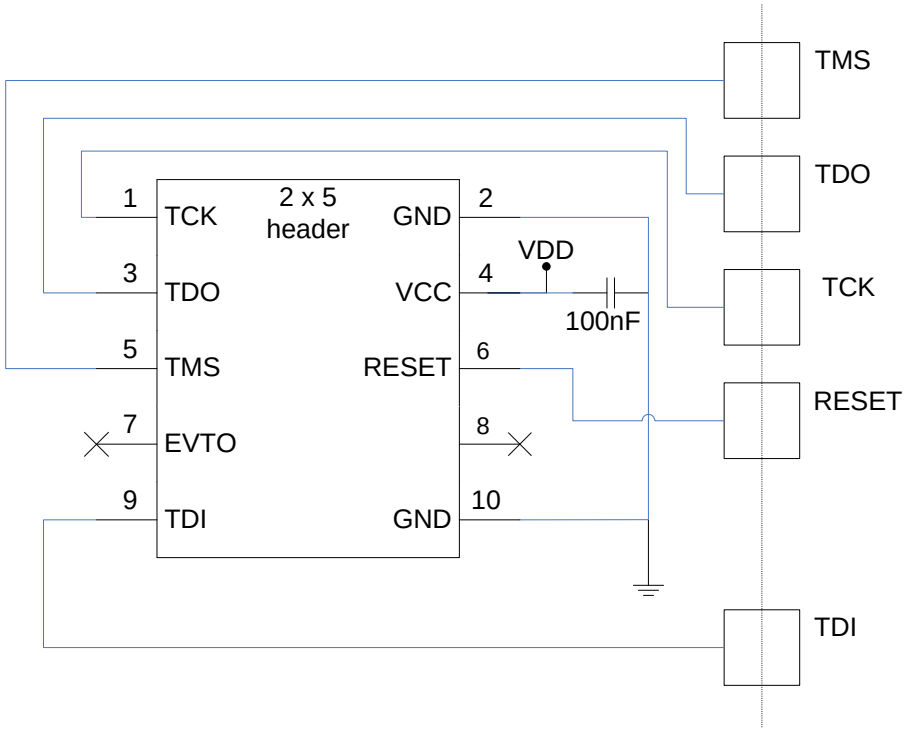

Table 6-1. JTAG port interface checklist

☑	Signal name	Recommended pin connection	Description
	TMS		Test mode select, sampled on rising TCK.
	TDO		Test data output, driven on falling TCK.
	TCK		Test clock, fully asynchronous to system clock frequency.
	RESET		Device external reset line.
	TDI		Test data input, sampled on rising TCK.
	EVTO		Event output, not used.

6.2 Nexus port interface

Figure 6-2. Nexus port interface example schematic

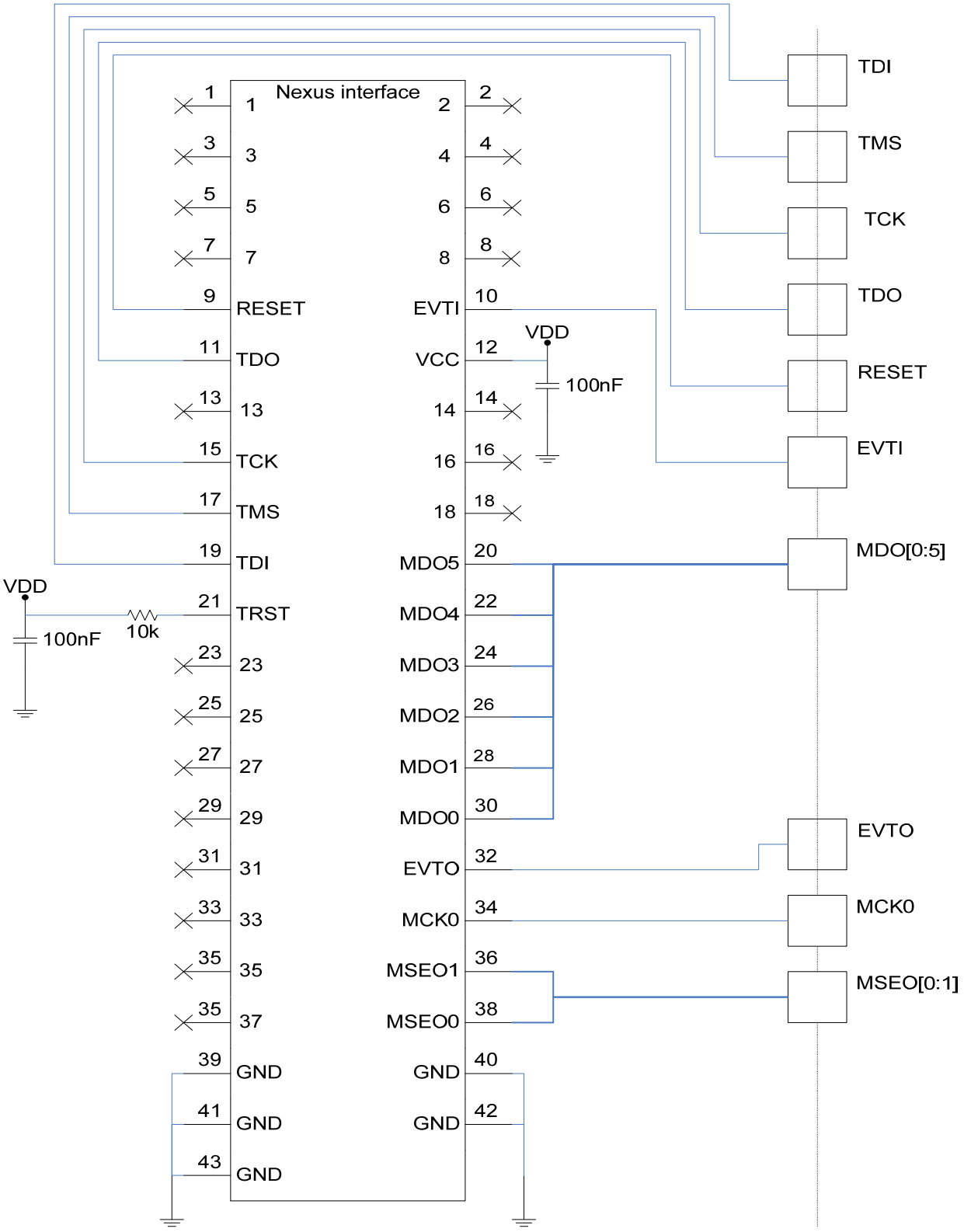

Table 6-2. Nexus port interface checklist

☑	Signal name	Recommended pin connection	Description
	TDI		Test data input, sampled on rising TCK.
	TMS		Test mode select, sampled on rising TCK.
	TCK		Test clock, fully asynchronous to system clock frequency.
	TDO		Test data output, driven on falling TCK.
	RESET		Device external reset line.
	EVTI		Event input.
	MDO[0:5](1)		Trace data output.
	EVTO		Event output.
	MCK0		Trace data output clock.
	MSE[0:1]		Trace frame control.

7 Suggested reading

7.1 Device datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. The datasheet is available on http://www.atmel.com/AVR32 in the *Datasheets* section.

7.2 Evaluation kit schematic

The evaluation kit EVK1101 contains the full schematic for the board; it can be used as a reference design. The schematic is available on http://www.atmel.com/AVR32 in the *Tools & Software* section.

Note that capacitors are soldered on the NEXUS trace data output lines on the EVK1101. This may cause speed limitations. In order to not have this limitation the capacitors has to be removed.

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