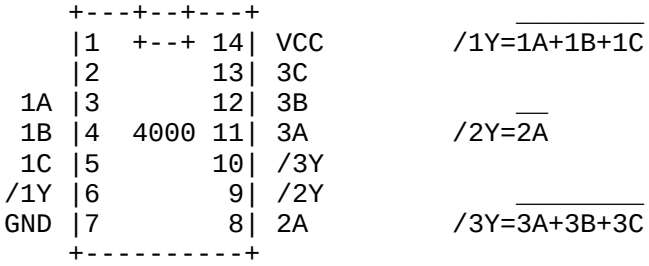
4000 series CMOS IC's: 4000...4049

The old but still much-used 4000 series logic IC's.

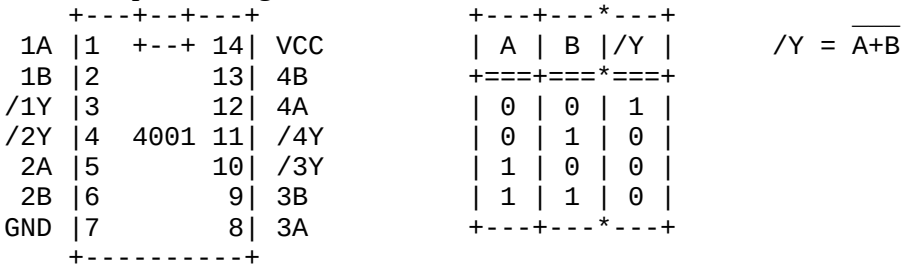
4000

Dual 3-input NOR gates and inverter.



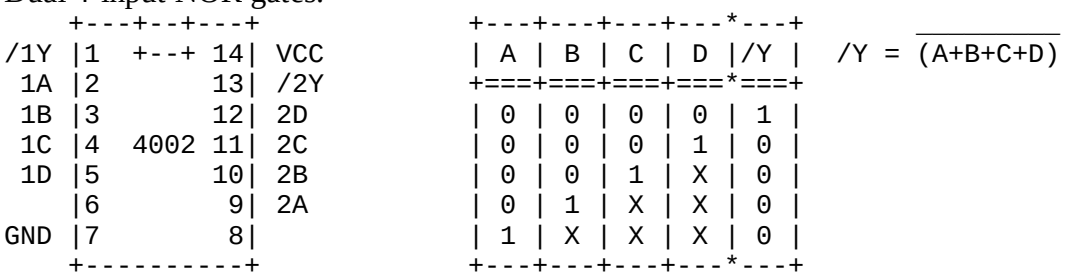
4001

Quad 2-input NOR gates.



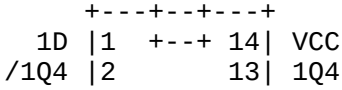
4002

Dual 4-input NOR gates.



4006

Dual 4-bit and dual 5-bit serial-in serial-out shift registers with common clock.



http://www.qsl.net/yo5ofh/data_sheets/4000.htm

```
 CLK |3       12| 2Q5
  2D |4  4006 11| 2Q4
  3D |5       10| 3Q4
  4D |6        9| 4Q5
 GND |7        8| 4Q4
     +----------+
```

4007

Dual complementary CMOS pair and unbuffered inverter.
For use as simple inverters, connect 1pS=3pS=VCC, 1nS=3nS=GND, 1pD=1nD=/1Y and 2pD=2nD=/2Y.

```
     +---+--+---+
 1pD |1  +--+ 14| VCC
 1pS |2       13| 2pD
  1G |3       12| /3Y
 1nS |4  4007 11| 3pS
 1nD |5       10| 3G
  2G |6        9| 3nS
 GND |7        8| 2nD
     +----------+
```

4008

4-bit binary full adder with fast carry.

```
    +---+--+---+
 A3 |1  +--+ 16| VCC         S=A+B+CIN
 B2 |2       15| B3
 A2 |3       14| CO
 B1 |4       13| S3
 A1 |5  4008 12| S2
 B0 |6       11| S1
 A0 |7       10| S0
GND |8        9| CI
    +----------+
```

4009

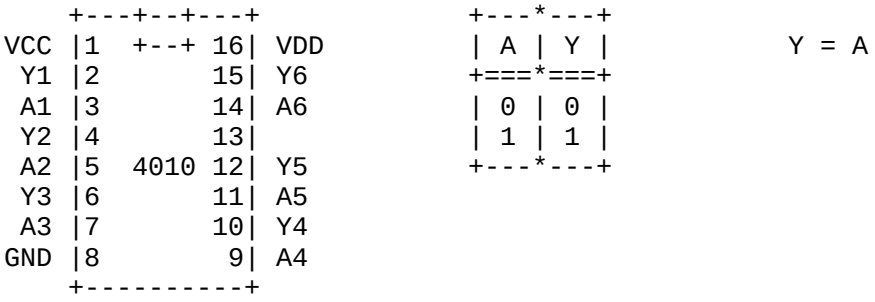
Hex inverters with level shifted outputs.
VDD may not be lower than VCC.

```
    +---+--+---+             +---*---+
VCC |1  +--+ 16| VDD         | A |/Y |          /Y = A
/Y1 |2       15| /Y6         +===*===+
 A1 |3       14| A6          | 0 | 1 |
/Y2 |4       13|             | 1 | 0 |
 A2 |5  4009 12| /Y5         +---*---+
/Y3 |6       11| A5
 A3 |7       10| /Y4
GND |8        9| A4
    +----------+
```

4010

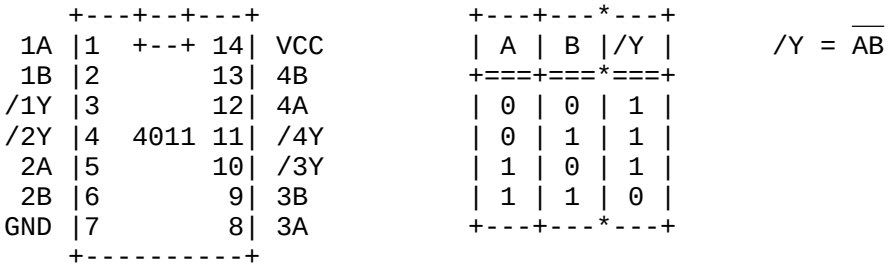
http://www.qsl.net/yo5ofh/data_sheets/4000.htm

Hex buffers with level shifted outputs.
VDD may not be lower than VCC.



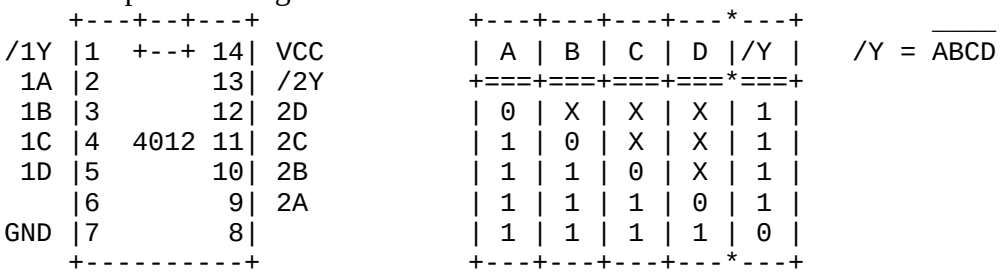
4011

Quad 2-input NAND gates.



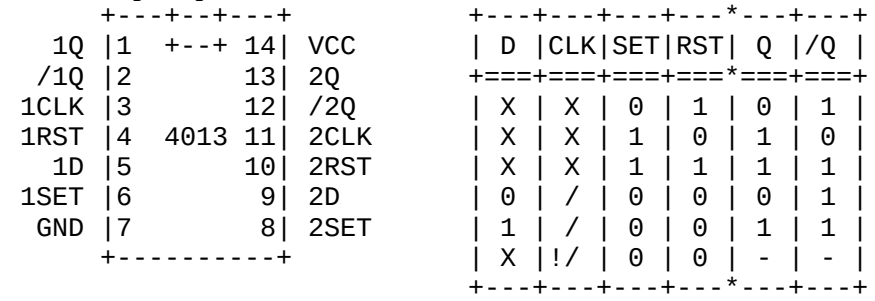
4012

Dual 4-input NAND gates.



4013

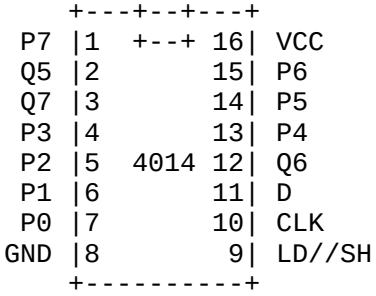
Dual D flip-flop with set and reset.



http://www.qsl.net/yo5ofh/data_sheets/4000.htm

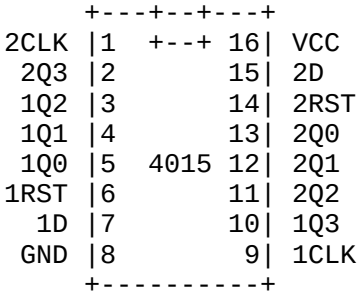
4014

8-bit parallel-in serial-out shift register with three parallel outputs.



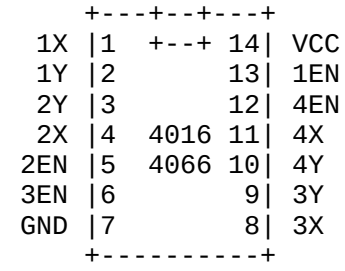
4015

Dual 4-bit serial-in parallel-out shift register with asynchronous reset.



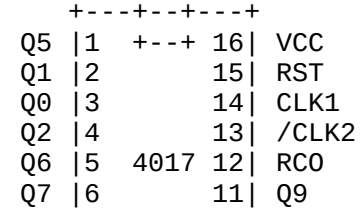
4016

Quad analog switches.



4017

4-bit asynchronous decade counter with fully decoded outputs, reset and both active high and active low clocks.



http://www.qsl.net/yo5ofh/data_sheets/4000.htm

```
 Q3 |7       10| Q4
GND |8        9| Q8
    +----------+
```

4018

5-stage (divide by 2,4,6,8 or 10) Johnson counter with preset inputs.

```
    +---+--+---+
  D |1  +--+ 16| VCC
 P1 |2       15| RST
 P2 |3       14| CLK
/Q2 |4       13| /Q5
/Q1 |5  4018 12| P5
/Q3 |6       11| /Q4
 P3 |7       10| PE
GND |8        9| P4
    +----------+
```

4019

8-to-4 line noninverting data selector/multiplexer with OR function.

```
    +---+--+---+
4A1 |1  +--+ 16| VCC
3A0 |2       15| 4A0
3A1 |3       14| S1
2A0 |4       13| Y4
2A1 |5  4019 12| Y3
1A0 |6       11| Y2
1A1 |7       10| Y1
GND |8        9| S0
    +----------+
```

```
+---+---+---+---*---+
| A0| A1| S1| S0| Y |    Y=S0.A0+S1.A1
+===+===+===+===*===+
| X | X | 0 | 0 | 0 |
| X | 0 | 0 | 1 | 0 |
| 0 | X | 1 | 0 | 0 |
| X | 1 | X | 1 | 1 |
| 1 | X | 1 | X | 1 |
+---+---+---+---*---+
```

4020

14-bit asynchronous binary counter with reset.
Q1 and Q2 outputs missing.

```
    +---+--+---+
Q11 |1  +--+ 16| VCC
Q12 |2       15| Q10
Q13 |3       14| Q9
 Q5 |4       13| Q7
 Q4 |5  4020 12| Q8
 Q6 |6       11| RST
 Q3 |7       10| /CLK
GND |8        9| Q0
    +----------+
```

4021

8-bit parallel-in serial-out shift register with asynchronous load input and three parallel outputs.

```
    +---+--+---+
```

http://www.qsl.net/yo5ofh/data_sheets/4000.htm

```
 P7 |1  +--+ 16| VCC
 Q5 |2       15| P6
 Q7 |3       14| P5
 P3 |4       13| P4
 P2 |5  4021 12| Q6
 P1 |6       11| D
 P0 |7       10| CLK
GND |8        9| LD//SH
    +----------+
```

4022

3-bit asynchronous binary counter with fully decoded outputs, reset and both active high and active low clocks.

```
    +---+--+---+
 Q1 |1  +--+ 16| VCC
 Q0 |2       15| RST
 Q2 |3       14| CLK1
 Q5 |4       13| /CLK2
 Q6 |5  4022 12| RCO
    |6       11| Q4
 Q3 |7       10| Q7
GND |8        9|
    +----------+
```

4023

Triple 3-input NAND gates.

```
    +---+--+---+             +---+---+---*---+
 1A |1  +--+ 14| VCC         | A | B | C |/Y |   /Y = ¯¯¯¯¯
 1B |2       13| 3C          +===+===+===*===+          ABC
 2A |3       12| 3B          | 0 | X | X | 1 |
 2B |4  4023 11| 3A          | 1 | 0 | X | 1 |
 2C |5       10| /3Y         | 1 | 1 | 0 | 1 |
/2Y |6        9| /1Y         | 1 | 1 | 1 | 0 |
GND |7        8| 1C          +---+---+---*---+
    +----------+
```

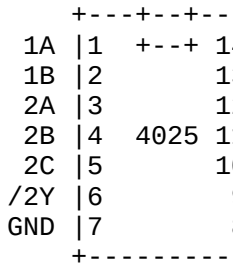
4024

7-bit asynchronous binary counter with reset.

```
     +---+--+---+
/CLK |1  +--+ 14| VCC
 RST |2       13|
  Q6 |3       12| Q0
  Q5 |4  4024 11| Q1
  Q4 |5       10|
  Q3 |6        9| Q2
 GND |7        8|
     +----------+
```

4025

Triple 3-input NOR gates.

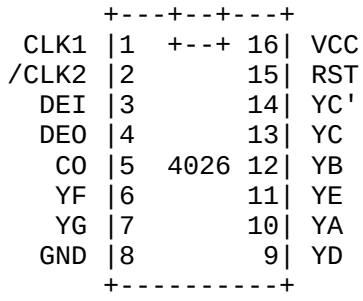


A	B	C	/Y
0	0	0	1
0	0	1	0
0	1	X	0
1	X	X	0

$$/Y = \overline{A+B+C}$$

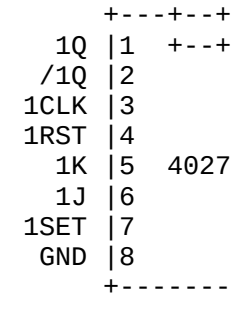
4026

4-bit asynchronous decade counter with 7-segment decoder/common-cathode LED driver, display enable, ripple carry, reset and both active high and active low clocks.



4027

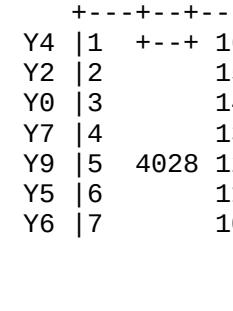
Dual J-K flip-flops with set and reset.



J	K	CLK	SET	RST	Q	/Q
X	X	X	1	1	1	1
X	X	X	1	0	1	0
X	X	X	0	1	0	1
0	0	/	0	0	-	-
0	1	/	0	0	0	1
1	0	/	0	0	1	0
1	1	/	0	0	/Q	Q
X	X	!/	0	0	-	-

4028

1-of-10 noninverting decoder/demultiplexer.



S3	S2	S1	S0	Y0	Y1	...	Y9
0	0	0	0	1	0	0	0
0	0	0	1	0	1	0	0
.	.	.	.	0	0	.	0
1	0	0	1	0	0	0	1
1	0	1	X	0	0	0	0

http://www.qsl.net/yo5ofh/data_sheets/4000.htm

```
GND |8        9| Y8
    +----------+
```

1	1	X	X	0	0	0	0

4029

4-bit synchronous binary/decade up/down counter with preset and ripple carry output.

```
     +---+--+---+
  PE |1  +--+ 16| VCC
  Q4 |2       15| CLK
  P4 |3       14| Q3
  P1 |4       13| P3
/RCI |5  4029 12| P2
  Q1 |6       11| Q2
/RCO |7       10| U//D
 GND |8        9| B//D
     +----------+
```

4030

Quad 2-input XOR gates.

```
    +---+--+---+
 1A |1  +--+ 14| VCC
 1B |2       13| 4B
 1Y |3       12| 4A
 2Y |4  4030 11| 4Y
 2A |5       10| 3Y
 2B |6        9| 3B
GND |7        8| 3A
    +----------+
```

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$Y = A \oplus B = (A.\overline{B})+(\overline{A}.B)$

4031

64-bit serial-in serial-out shift register with multiplexed inputs.
Y is Q63 delayed by half a cycle (i.e. clocked on falling edge).

```
     +---+--+---+
   E |1  +--+ 16| VCC
 CLK |2       15| D
     |3       14|
     |4       13|
   Y |5  4031 12|
 Q63 |6       11|
/Q63 |7       10| E//D
 GND |8        9| CLKout
     +----------+
```

4032

Triple serial adder.
Each section can be used to add long binary words, one bit on each clock cycle. CRST resets the internal carry flip-flop after one clock delay. The INV inputs can be used to invert the sum output (giving a 1's-complemented result).

```
     +---+--+---+
```

http://www.qsl.net/yo5ofh/data_sheets/4000.htm

```
  3S |1  +--+ 16| VCC
3INV |2       15| 3A
 CLK |3       14| 3B
  2S |4       13| 2A
2INV |5  4032 12| 2B
CRST |6       11| 1B
1INV |7       10| 1A
 GND |8        9| 1S
     +----------+
```

4033

4-bit asynchronous decade counter with 7-segment decoder/common-cathode LED driver, ripple blanking, ripple carry, reset and both active high and active low clocks.

```
      +---+--+---+
 CLK1 |1  +--+ 16| VCC
/CLK2 |2       15| RST
  RBI |3       14| LT
  RBO |4       13| YC
   CO |5  4033 12| YB
   YF |6       11| YE
   YG |7       10| YA
  GND |8        9| YD
      +----------+
```

4034

8-bit bidirectional universal shift register with common serial input, dual parallel I/O ports and selectable synchronous/asynchronous parallel load.

```
     +-----+--+-----+
  A7 |1    +--+   24| VCC
  A6 |2           23| B7
  A5 |3           22| B6
  A4 |4           21| B5
  A3 |5           20| B4
  A2 |6           19| B3
  A1 |7    4034   18| B2
  A0 |8           17| B1
 ENA |9           16| B0
   D |10          15| CLK
B//A |11          14| SY//ASY
 GND |12          13| LD//SH
     +--------------+
```

4035

4-bit inverting/noninverting universal shift register with J-/K inputs and asynchronous reset.

```
       +---+--+---+
    Q0 |1  +--+ 16| VCC
  /INV |2       15| Q1
    /K |3       14| Q2
     J |4       13| Q3
```

http://www.qsl.net/yo5ofh/data_sheets/4000.htm

```
   RST |5  4035 12| P3
   CLK |6       11| P2
LD//SH |7       10| P1
   GND |8        9| P0
       +----------+
```

4038

Triple negative-edge-triggered serial adder.
Each section can be used to add long binary words, one bit on each clock cycle. CRST resets the internal carry flip-flop after one clock delay. The INV inputs can be used to invert the sum output (giving a 1's-complemented result).

```
     +---+--+---+
  3S |1  +--+ 16| VCC
3INV |2       15| 3A
/CLK |3       14| 3B
  2S |4       13| 2A
2INV |5  4038 12| 2B
CRST |6       11| 1B
1INV |7       10| 1A
 GND |8        9| 1S
     +----------+
```

4040

12-bit asynchronous binary counter with reset.

```
    +---+--+---+
Q11 |1  +--+ 16| VCC
 Q5 |2       15| Q10
 Q4 |3       14| Q9
 Q6 |4       13| Q7
 Q3 |5  4040 12| Q8
 Q2 |6       11| RST
 Q1 |7       10| /CLK
GND |8        9| Q0
    +----------+
```

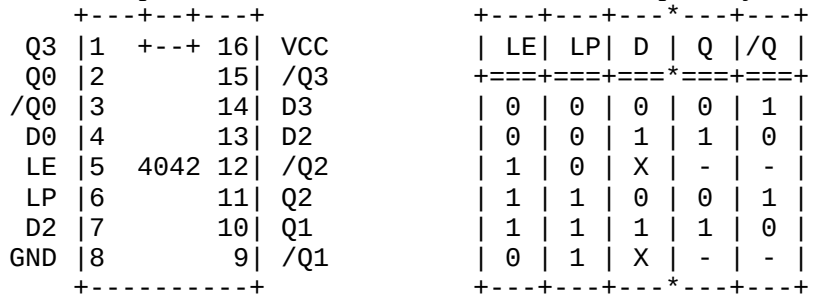
4041

Quad buffers with complementary outputs.

```
    +---+--+---+             +---*---+---+
 1Y |1  +--+ 14| VCC         | A | Y |/Y |       Y = A
/1Y |2       13| 4A          +===*===+===+
 1A |3       12| /4Y         | 0 | 0 | 1 |
 2Y |4  4041 11| 4Y          | 1 | 1 | 0 |
/2Y |5       10| 3A          +---*---+---+
 2A |6        9| /3Y
GND |7        8| 3Y
    +----------+
```

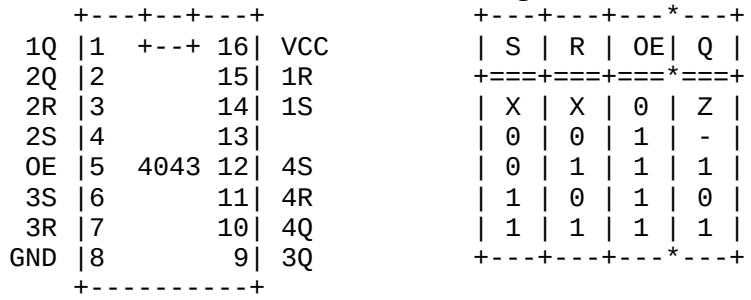
4042

4-bit transparent latch with selectable latch enable polarity and complementary outputs.



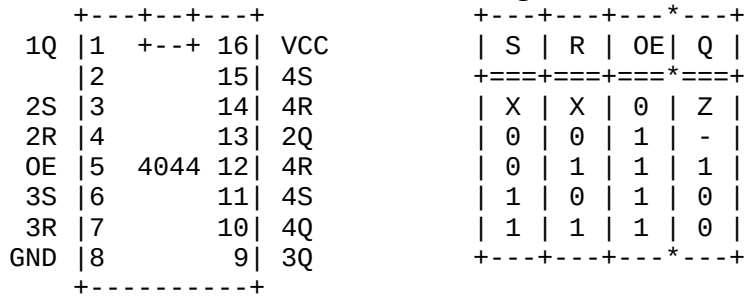
4043

Quad 3-state S-R latches with overriding set.



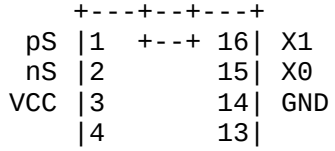
4044

Quad 3-state S-R latches with overriding reset.



4045

21-bit asynchronous binary counter with oscillator and reset input.
Only two 3% duty cycle outputs (180` out of phase) from the last counter stage are available. Can be used to generate a 1Hz clock signal using a 2.097152MHz crystal. P and N MOSFET source connections from the oscillator inverter are brought out of the package to allow the use of source resistors, but usually pS=VCC and nS=GND.



```
    |5  4045 12|
    |6       11|
 QA |7       10|
 QB |8        9|
    +----------+
```

4046

Phase Locked Loop.

```
       +---+--+---+
PCPout |1  +--+ 16| VCC
PC1out |2       15| Zener
 PCinB |3       14| PCinA
VCOout |4       13| PC2out
   /EN |5  4046 12| R2
   C1A |6       11| R1
   C1B |7       10| SFout
   GND |8        9| VCOin
       +----------+
```

4047

Low-power astable/monostable multivibrator with oscillator output.

```
      +---+--+---+
 Cext |1  +--+ 14| VCC
 Rext |2       13| OSC
RCext |3       12| RETRIG
 /AST |4  4047 11| /Q
  AST |5       10| Q
  /TR |6        9| RST
  GND |7        8| TR
      +----------+
```

4048

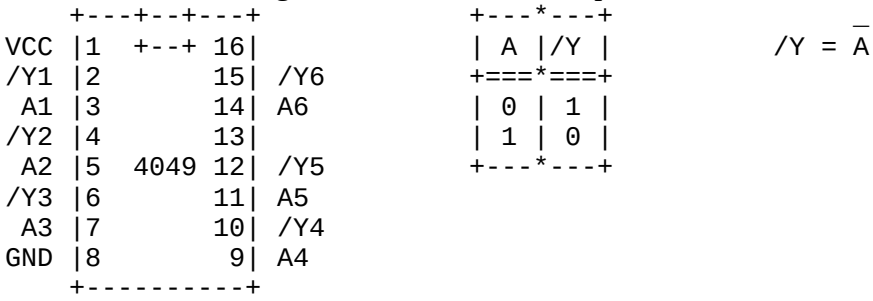
3-state 8-input multifunction gate.

```
    +---+--+---+
  Y |1  +--+ 16| VCC
 OE |2       15| X
  A |3       14| H
  B |4       13| G
  C |5  4048 12| F
  D |6       11| E
 S1 |7       10| S2
GND |8        9| S0
    +----------+
```

S2	S1	S0	OE	Output function
X	X	X	0	Z
0	0	0	1	8-input NOR
0	0	1	1	8-input OR
0	1	0	1	2-wide 4-input OR-AND
0	1	1	1	2-wide 4-input OR-NAND
1	0	0	1	8-input AND
1	0	1	1	8-input NAND
1	1	0	1	2-wide 4-input AND-NOR
1	1	1	1	2-wide 4-input AND-OR

4049

Hex inverters with high-to-low level shifter inputs.



4066

Quad analog switches.